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Term: (microprocessor$ same memory$ same clock$ same fabricat$ same substrate$)

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L1	(integrate$ adj circuit).ab.	25916	L1

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	DB=USPT; PLUR=YES; OP=ADJ		
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L2	L1 and (microprocessor$ same memory$ same clock$ same fabricat$ same substrate$)	0	L2
L1	(integrate$ adj circuit).ab.	25916	L1

END OF SEARCH HISTORY

L3: Entry 1 of 5 File: USPT May 29, 2001

DOCUMENT-IDENTIFIER: US 6239510 B1
TITLE: Reduced impact power up/down mode in electrical circuits

Brief Summary Text (4):
Most electrical circuits produced today are fabricated on a single substrate known as an integrated circuit (IC) chip. These IC chips are often interconnected via further substrates, such as printed circuit boards. The IC chips are typically connected to each other by metal traces formed on the surface of the circuit boards. The IC chips may include active devices such as logic circuitry or memory cells. The plurality of IC chips on the circuit board are typically controlled by a microprocessor or central processing unit (CPU) which may or may not be disposed on the board. The circuit board also usually includes a clock generator and a voltage source, both of which may alternatively be located off circuit board. The clock generator and the voltage source produce signals which are applied to the IC chips to make them operate. The IC chips along with the CPU and other associated discrete circuit elements form a circuit device for effecting a particular task.

L3: Entry 5 of 5 File: USPT Sep 20, 1983

DOCUMENT-IDENTIFIER: US 4406013 A
TITLE: Multiple bit output dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

L3: Entry 2 of 5 File: USPT Dec 12, 2000

DOCUMENT-IDENTIFIER: US 6161167 A
TITLE: Fully associate cache employing LRU groups for cache replacement and mechanism for selecting an LRU group

Detailed Description Text (5):
Generally speaking, microprocessor 10 includes an L0 cache 26 for providing load memory operation data or receiving store memory operation data during a clock cycle in which execute units 18 provide the address corresponding to the memory operation. L0 cache 26 is relatively small as compared to data cache 14. For example, L0 cache 26 may comprise between 32 and 64 cache line storage locations as compared to 1024 cache line storage locations in data cache 14, according to one embodiment. Other embodiments may include more or fewer cache line storage locations. Due to its relatively small size, L0 cache 26 may be physically located near execute units 18 upon a semiconductor substrate upon which microprocessor 10 is fabricated. Interconnect delay between L0 cache 26 and execute units 18 may thereby be lessened. Furthermore, the small size of L0 cache 26 engenders a relatively low cache latency. Advantageously, overall cache latency (and load to use penalties) may be reduced when a hit in L0 cache 26 is detected.

L3: Entry 3 of 5 File: USPT Oct 15, 1985

DOCUMENT-IDENTIFIER: US 4547867 A
TITLE: Multiple bit dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

L3: Entry 4 of 5 File: USPT Jun 5, 1984

DOCUMENT-IDENTIFIER: US 4453237 A
TITLE: Multiple bit output dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

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☐ 1. Document ID: US 4547867 A

L4: Entry 1 of 3 File: USPT Oct 15, 1985

DOCUMENT-IDENTIFIER: US 4547867 A
TITLE: Multiple bit dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

Detailed Description Text (11):
The internal data/address bus 28, in addition to being coupled to the gates 30 and 31, is coupled to the data-out buffers 26, the data-in buffers 25 and the row address latches 24. This bus also couples the address signals A.sub.0 -A.sub.5 (and A.sub.12 if A.sub.0 is not used for an address) to the row decoders. The column address latches 23 are coupled through the bus 27 to the column decoders 16 and 17. The other control signals associated with the memory are coupled either to the arbitration, refresh logic, timing and control means 33 or to the latches 37.

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☐ 2. Document ID: US 4453237 A

L4: Entry 2 of 3 File: USPT Jun 5, 1984

DOCUMENT-IDENTIFIER: US 4453237 A
TITLE: Multiple bit output dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

Detailed Description Text (11):
The internal data/address bus 28, in addition to being coupled to the gates 30 and 31, is coupled to the data-out buffers 26, the data-in buffers 25 and the row address latches 24. This bus also couples the address signals A.sub.0 -A.sub.5 (and A.sub.12 if A.sub.0 is not used for an address) to the row decoders. The column address latches 23 are coupled through the bus 27 to the column decoders 16 and 17. The other control signals associated with the memory are coupled either to the arbitration, refresh logic, timing and control means 33 or to the latches 37.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 4406013 A

L4: Entry 3 of 3 File: USPT Sep 20, 1983

DOCUMENT-IDENTIFIER: US 4406013 A
TITLE: Multiple bit output dynamic random-access memory

Detailed Description Text (4):
In its presently preferred embodiment, the described memory is realized as a 4K.times.8 array, disposed on a silicon substrate with all peripheral circuits such as buffers, decoders, etc. The memory is fabricated with n-channel MOS field-effect transistors employing double layers of polycrystalline silicon. A single power supply of +5 volts is used, with on-chip generation of a substrate biasing potential of approximately -3 volts. The memory consumes approximately 250 milliwatts when active and 50 milliwatts in stand-by modes. Typical access time is 200 ns, making the memory compatible with the 8 MHz clock rate of commercial microprocessors such as the Intel 8086.

Detailed Description Text (11):
The internal data/address bus 28, in addition to being coupled to the gates 30 and 31, is coupled to the data-out buffers 26, the data-in buffers 25 and the row address latches 24. This bus also couples the address signals A.sub.0 -A.sub.5 (and A.sub.12 if A.sub.0 is not used for an address) to the row decoders. The column address latches 23 are coupled through the bus 27 to the column decoders 16 and 17. The other control signals associated with the memory are coupled either to the arbitration, refresh logic, timing and control means 33 or to the latches 37.

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